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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/816,118
Filing Date: April 01, 2004
Appellant(s): PAI ET AL.

Mirut P. Dalal
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/24/10 appealing from the Office action mailed 10/23/09.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-3, 5, 7-9 and 15 are rejected and pending in the current application.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the

subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

6,310,921	Yoshioka	10-2001
5,706,059	Ran et al.	01-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1-3, 5, 7-9, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (Yoshioka) US 6,310,921 B1 in view of Ran et al. (Ran) US 5,706,059.

2. As to claim 1, Yoshioka teaches a video request manager [Fig. 3; Fig. 4; Fig. 16] comprising: a first state machine for commanding a memory controller to fetch reference pixels for a first portion of a picture; [Fig. 4; Fig. 16; Col. 11 Line 64 – Col. 12 Line 7; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14] and a second state machine for commanding a memory controller to write a second portion of the picture, [Fig. 4; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14, 20-27] memory controller fetches the reference pixels. [Col. 14 Lines 38-45]

Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem.

However, Yoshioka is silent as to the second state machine loads the memory controller with the second portion while the memory controller fetches as claimed.

Ran teaches the second state machine loads the memory controller with the second portion while the memory controller fetches. [abstract; col. 3 lines 4-10]

It would have been obvious at the time the invention was made to incorporate the simultaneous read/search and write teachings of Ran with the device of Yoshioka allowing for efficiency in image coding.

3. As to claim 2, Yoshioka (modified Ran) teaches the second state machine commands the memory controller to write the second portion, such that a resource contention occurs between the command to fetch reference pixels, and the command to write the second portion. [Yoshioka - Fig. 3; Fig. 4]

4. As to claim 3, Yoshioka (modified Ran) teaches the second state machine commands the memory controller to write the second portion, such that the command to fetch reference pixels is given priority during the resource contention. [Yoshioka - Col. 11 Lines 39-41; Col. 14 Lines 38-45]

5. As to claim 5, Yoshioka teaches a circuit for decoding video data, [Fig. 4 (1002); Col. 11 Lines 30-41; Col. 12 Line 62 – Col. 13 Line 4] said circuit comprising: a motion vector address computer for calculating at least one address for reference pixels for a first portion of a picture; [Col. 5 Lines 62-64; Col. 5 Line 67 Col. 6 Line 2; Fig. 6; Col. 14 Lines 38-45; Col. 13 Lines 66-67; Fig. 10; Col. 18 Lines 9-14; Fig. 21 Fig. 19; Col. 16 Lines 26-54] a motion compensator for decoding another portion of the picture; [Col. 15

Line 65 – Col. 16 Line 2; Fig. 15 (A&B); Col. 23 Lines 62-67] and a video request manager comprising: a first state machine for issuing a command to fetch reference pixels for a first portion of a picture; [Fig. 4; Fig. 16; Col. 11 Line 64 – Col. 12 Line 7; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14] and a second state machine for issuing a command to write a second portion of the picture. [Fig. 4; Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14, 20-27] a memory controller fetching the reference pixels after the first state machine issues the command, and writing the second portion of the picture after the second state machine issues the command. [Col. 15 Line 65 –Col. 16 Line 2; Fig. 15 (A&B); Col. 23 Lines 62-67]

Yoshioka teaches pipeline processing in decoding including read/write function that is divided into two sections [see fig. 15 A&B] allowing them to operate in tandem. However, Yoshioka is silent as to memory controller loads the second portion of the picture while fetching as claimed.

Ran teaches the memory controller loads the second portion of the picture while fetching. [abstract; col. 3 lines 4-10]

It would have been obvious at the time the invention was made to incorporate the simultaneous read/search and write teachings of Ran with the device of Yoshioka allowing for efficiency in image coding.

6. As to claim 7, Yoshioka (modified Ran) teaches the memory controller [Fig. 4 (6); Fig. 16 (26)] further comprises: an arbiter for causing the memory controller to give

priority to the command to fetch the reference pixels. [Yoshioka - Col. 11 Lines 39-41; Col. 14 Lines 38-45]

7. As to claim 8, Yoshioka (modified Ran) teaches the memory controller [Fig. 4 (6); Fig. 16 (26)] further comprises: a write buffer for storing the second portion of the picture while fetching the reference pixels. [Yoshioka - Col. 13 Line 56 – Col. 14 Line 4; Fig. 10; Col. 18 Lines 6-14]

8. As to claim 9, Yoshioka (modified Ran) teaches the memory controller [Fig. 4 (6); Fig. 16 (26)] writes the second portion of the picture from the write buffer to a memory system, after fetching the reference pixels. [Yoshioka - Col. 11 Lines 39-41; Col. 14 Lines 38-45]

9. As to claim 15, Yoshioka (modified Ran) teaches the second state machine loads the memory controller with the second portion reconstructed from decoding while the memory controller fetches the reference pixels. [Ran - abstract; col. 3 lines 4-10]

(10) Response to Argument

Argument: claims 1 and 5

The Examiner respectfully disagrees with the Applicant's statement. The rejection of claims 1 and 5 should be maintained being that the combination of Yoshioka and Ran fairly suggests and teaches the limitations as claimed. The cited references of Yoshioka and Ran can be combined in the manner presented within the office action.

A. The rejection to claim1 should be reversed because the combination of Yoshioka and Ran does not teach "fetching reference pixels for a first portion of a picture" and "loads the memory controller with the second portion while the memory controller fetches the reference pixels".

The Examiner disagrees with the Applicant's arguments. Yoshioka taken in combination with Ran teaches the limitations of claims 1 and 5. Yoshioka discloses a media processing device that compresses and decompresses audio/visual data. [abstract; col. 1 lines 8-11] The device taught by Yoshioka processes information on a block by block basis at the pixel level using the MPEG standard. [fig. 4; col. 10 lines 13-23; col. 11 lines 52-59] Yoshioka uses local search teach technique in its motion compensation. The pixel read/write extracts the rectangular local search area not entire frame or picture when performing motion compensation. The local search area retrieved is a portion of the current frame. [Col. 11 Line 64 – Col. 12 Line 7; Col. 13 Line 56 – Col. 14 Line 4; col. 14 lines 38-45; Col. 18 Lines 6-27] Yoshioka teaches that in the alternative motion estimation circuit could be used where the motion vectors of the already calculated blocks of the preceding and succeeding frames are used as reference frames. [col. 27 lines 5-18] However that embodiment was not cited by the Examiner. The local search disclosed within Yoshioka uses a portion of the present frame for motion calculations, where the data is stored and retrieved from the memory. [col. 14 lines 38-45; col. 18 Lines 6-27] Ran discloses a motion estimation device which writes to a memory while (i.e. simultaneously) reading from another part of the memory. [abstract; col. 3 lines 4-10] Ran retrieves search data from the other two parts of the

memory this is equivalent to a read operation. The loading of a portion of memory as disclosed by Ran is equivalent to a writing operation. The cited prior art Yoshioka taken in combination with Ran teaches the Applicant's limitations as claimed.

B. The rejection of claim 1 should be reversed because it would not obvious to modify Yoshioka with the teachings of Ran

The Examiner disagrees with the Applicant's arguments. Yoshioka and Ran are within the same field of endeavor. Yoshioka teaches the storage of motion data within a memory which can be loaded to and read from. Ran teaches motion estimation using search data where the data is stored within a memory. The memory function of simultaneous read/write of Ran is used to modify the Yoshioka. It would have been obvious at the time the invention was made to incorporate the simultaneous read/search and write teachings of Ran with the device of Yoshioka allowing for efficiency in image processing.

In response to applicant's argument that it would not be obvious to modify Yoshioka with the teachings of Ran to perform simultaneous read/write to a memory, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/Anner Holder/

Examiner, Art Unit 2483

Conferees:

/Joseph G Ustaris/

Supervisory Patent Examiner, Art Unit 2483

/Mehrdad Dastouri/

Quality Assurance Specialist, TC 2400